EE-281 Logic Design Lab

Lab #4

Alarm System

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# **Introduction**

This Lab primarily focuses on building a top down design of an advanced alarm system. The design will be made such that it protects two doors by using different security alert levels and password override protection system. Initially we are required to design a logical circuit followed by testing it with FPGA board by using Verilog. When the tests were approved we designed the circuit and implemented it on the protoboard.

# **Experiment Description**

The group initially considered the six inputs of the logic system and made a truth table out of it. We were given 4 different security alert levels which are as below:

* A1 A0 Level
* 0 0 Off
* 0 1 Low Alert
* 1 1 High Alert
* 1 0 not defined

Along with a Password override bit and two door sensors make up the inputs. When PO is activated it is 1, otherwise it is zero. Then we designed the truth table according these conditions which were given to us.

Truth Table 1

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| D1 | D2 | PO | A1 | A0 | X1 | X0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | d | d |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | d | d |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | d | d |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | d | d |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | d | d |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | d | d |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | d | d |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | d | d |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |

We used the above truth table to design the logic using KMAP and then minimized the equation obtained from the KMAP. This equation was then used to design the circuit. We used 5 input KMAP for the two outputs Xo and X1 which was then used to design the circuit.

Below is the Karnaugh Map for the previous truth table (X1):

D1=0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | D2P0 |  |  |  |  |
| A1A0 |  | 00 | 01 | 11 | 10 |
|  | 00 | 0 | 0 | 0 | 0 |
|  | 01 | 0 | 0 | 0 | 1 |
|  | 11 | 0 | 0 | 1 | 1 |
|  | 10 | d | d | d | d |

D1 = 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | D2P0 |  |  |  |  |
| A1A0 |  | 00 | 01 | 11 | 10 |
|  | 00 | 0 | 0 | 0 | 0 |
|  | 01 | 1 | 0 | 0 | 1 |
|  | 11 | 1 | 1 | 1 | 1 |
|  | 10 | d | d | d | d |

Below is the Karnaugh Map for the previous truth table (X0):

D1=0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | D2P0 |  |  |  |  |
| A1A0 |  | 00 | 01 | 11 | 10 |
|  | 00 | 0 | 0 | 0 | 0 |
|  | 01 | 0 | 0 | 0 | 0 |
|  | 11 | 1 | 1 | 0 | 1 |
|  | 10 | d | d | d | d |

D1 = 1

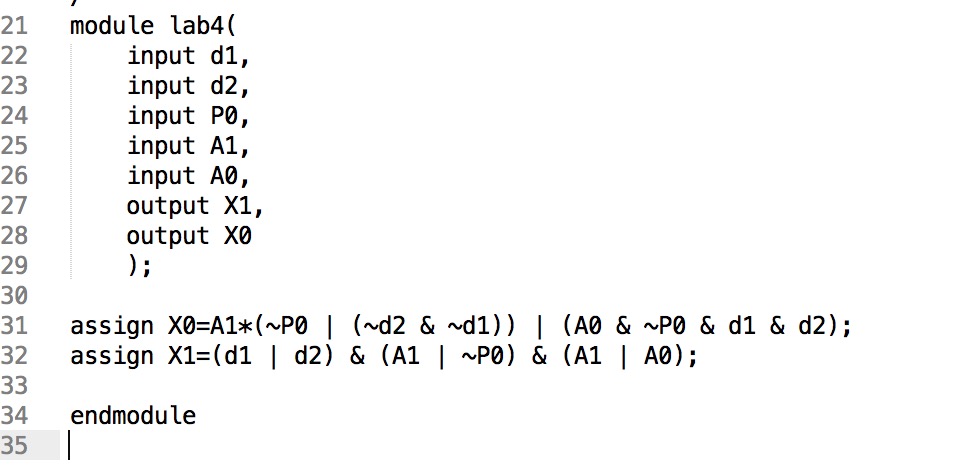
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | D2P0 |  |  |  |  |
| A1A0 |  | 00 | 01 | 11 | 10 |
|  | 00 | 0 | 0 | 0 | 0 |
|  | 01 | 0 | 0 | 0 | 1 |
|  | 11 | 1 | 0 | 0 | 1 |
|  | 10 | d | d | d | d |

Using the above Karnaugh Maps we derived the following equations for X0 and X1:

X0 = A1 & (~P0 | (~d2 & d1)) | (A0 & ~P0 & d1 & d2)

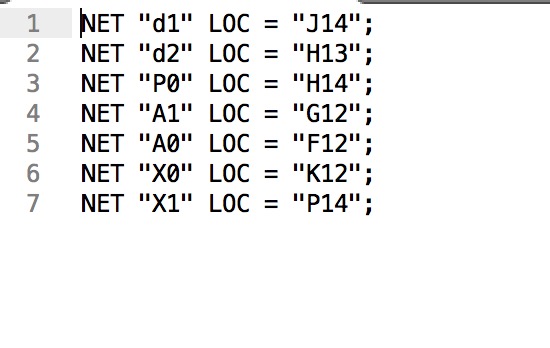
X1 = (d1 | d2) & (A1 | ~P0) & (A1 | A0)

Now before building the circuit of X0 and X1 from the equation obtained from the KMAP above. We first test if our design equation are correct or not by using the FPGA programming board and Verilog.

Given below is the Verilog code for the equation which was built by using the KMAPS.

Verilog Code 1

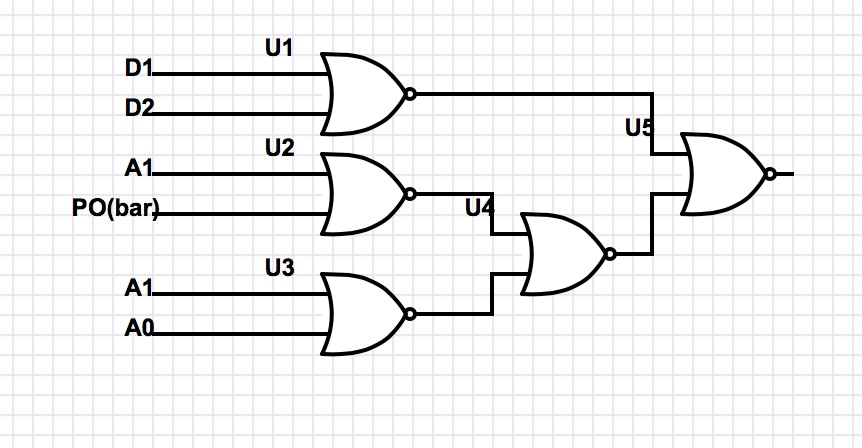
UCF File 1



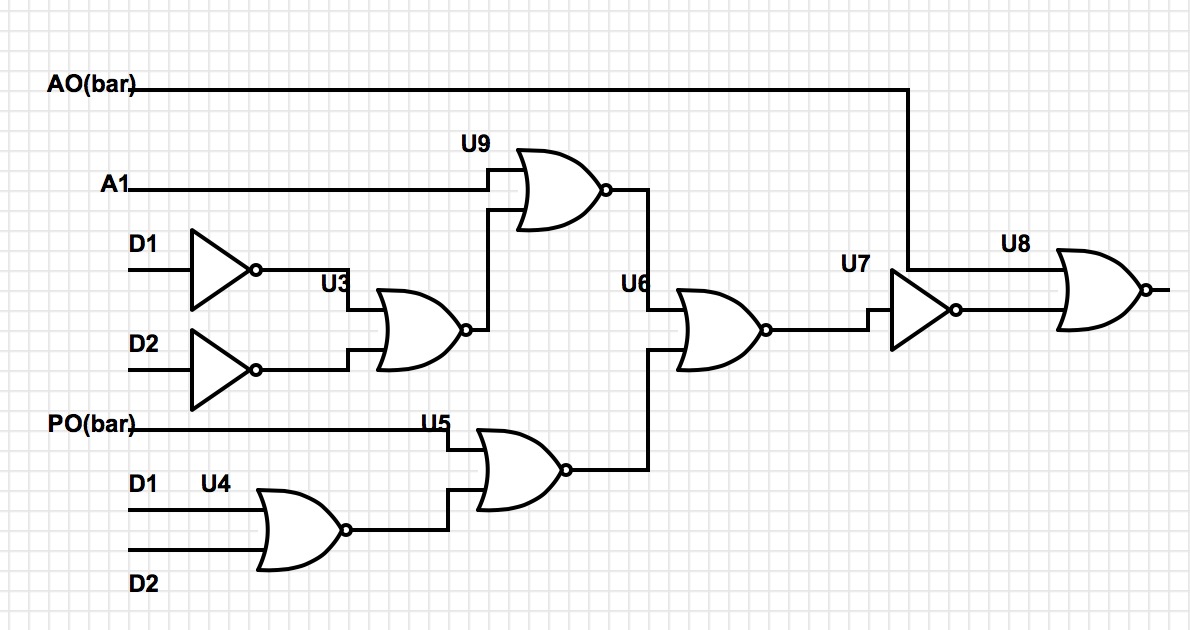
From these test results we came to the understanding that the design for the circuit works and we later

The design for the two bits of the Alert Levels X0 and X1 is shown below.

## DESIGN FOR X1



## DESIGN FOR X0



# **Results**

The results of this experiment came to a successful approach since the experiment was designed properly by the team. The team did multiple error checking on the logic circuit after testing with FPGA Programmable board. The circuit did have minor issues. After testing the circuit with FPGA board when we implemented the design there was errors involved in some of the bits not displaying any output. The team used to logic probe to rectify the errors in the circuit and then we were able to successfully get the desired output.

The security levels were correctly displayed on the seven segment display according to the different values we input into the truth table. The result of the advanced alarm systems correctly outputs the 4 different levels of security when they were triggered.

# **Conclusion**

In conclusion, this lab taught us a lot about the design process. The system we are designing in this lab could translate easily into a practical application. This lab emphasized the design process. While for the most part we did well, in future labs we should triple check our answers in the design process to help us when we make it to the lab. In addition, this lab taught us how to properly test our circuit for errors. When we wired up the circuit, we made a mistake in the wiring which cost us about an hour of debug time. While not ideal, it was very helpful in making us understand the importance of triple checking the wires at each stage of the building process and taught us how to assess what went wrong. All in all, this lab contributed to our understanding of the material perhaps more than the first three.